TS32MLR72V8D2

168 PIN PC100 Registered DIMM
256MB With 16M X 8 CL2

Description

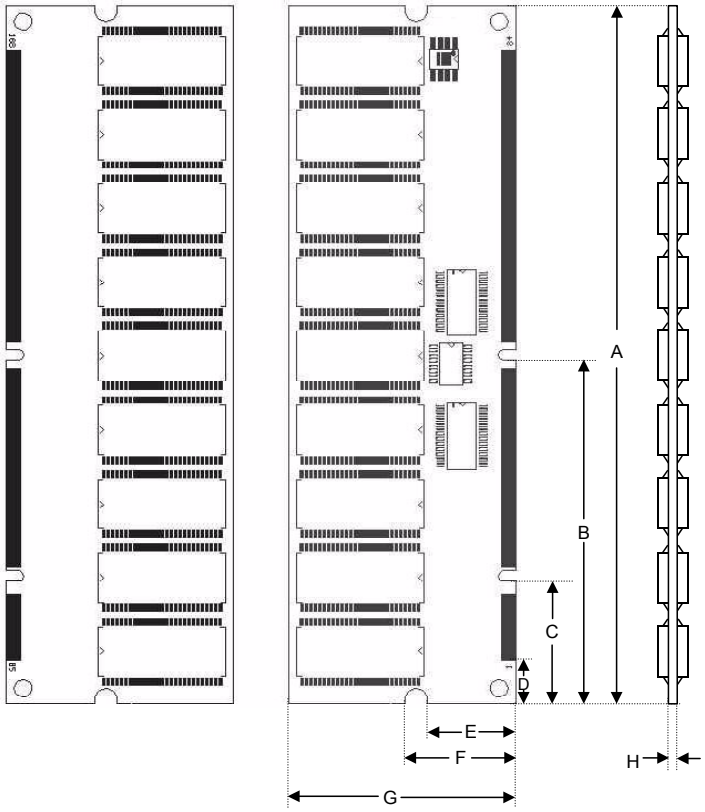
The TS32MLR72V8D2 is a 32M bit x 72 Synchronous Dynamic RAM high-density memory registered DIMM module. The TS32MLR72V8D2 consists of 18pcs of CMOS 16Mx8bits Synchronous DRAMs in TSOP-II 400mil packages, 2pcs of drive ICs, 1pc of PLL and one 2048 bits serial EEPROM on a 168-pin printed circuit board. The TS32MLR72V8D2 is a Dual In-Line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Performance Range: PC-100 CL2.
- Burst Mode Operation.
- Auto and Self Refresh.
- Serial Presence Detect (SPD) with serial EEPROM
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8 & Full Page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

Placement



PCB: 09-7395

Dimensions

Side	Millimeters	Inches
A	133.35±0.400	5.250±0.016
B	65.67	2.585
C	23.49	0.925
D	8.89	0.350
E	15.78	0.621
F	19.78	0.778
G	40.50±0.200	1.594±0.008
H	1.27±0.100	0.050±0.004

(Refer Placement)

Pin Identification

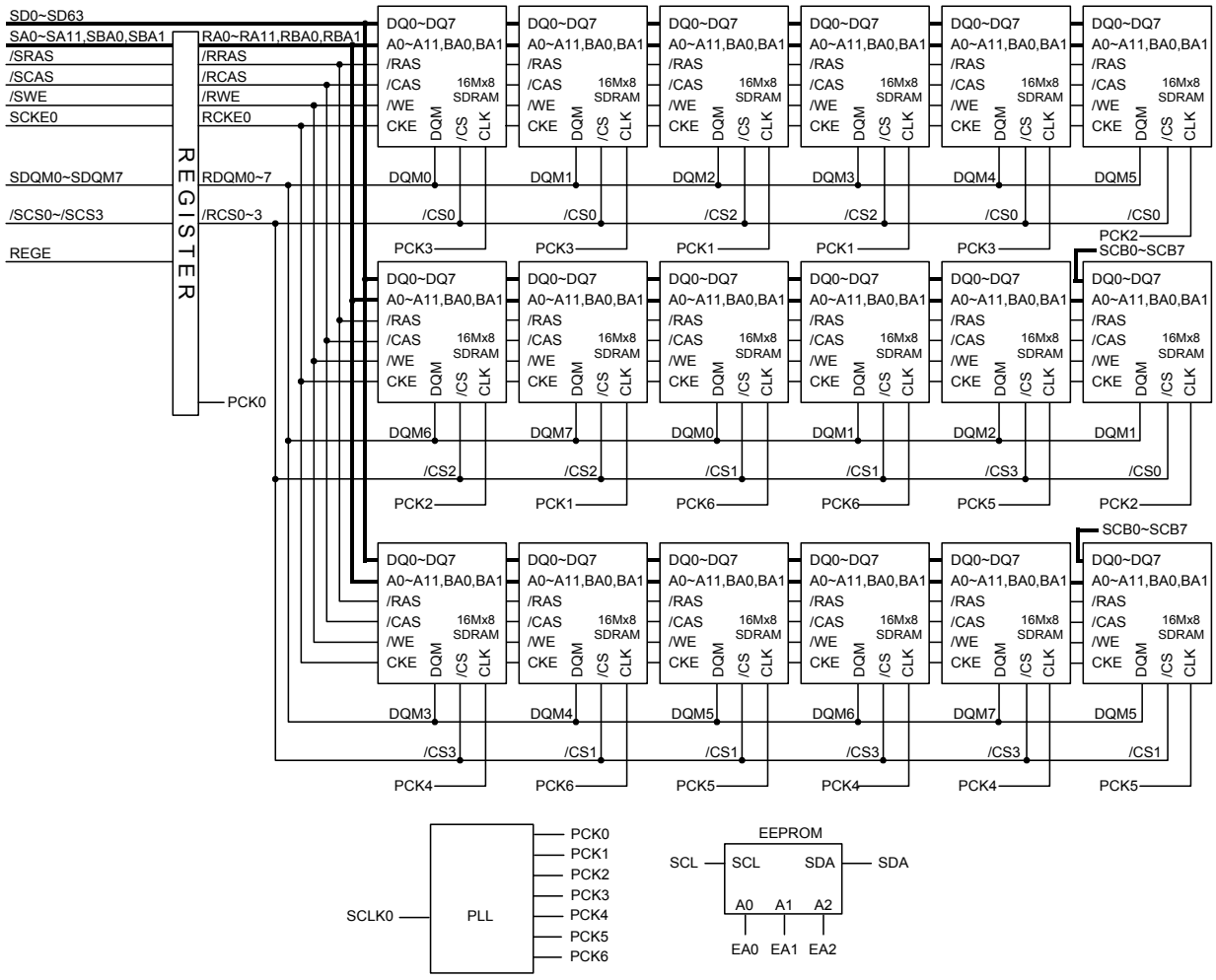
Symbol	Function
SA0~SA11	Address Input
SBA0, SBA1	Select Bank Address
SD0~SD63	Data Input / Output.
SCB0~SCB7	Check bit (data-in / data-out)
SCLK0	Clock Input.
SCKE0	Clock Enable Input.
/SCS0~/SCS3	Chip Select Input.
/SRAS	Row Address Strobe
/SCAS	Column Address Strobe
/SWE	Write Enable
SDQM0~SDQM7	Data (DQ) Mask
REGE	Register Enable
EA0~EA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
Vcc	+3.3 Voltage Power Supply
Vss	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	43	Vss	85	Vss	127	Vss
02	SDQ0	44	NC	86	SDQ32	128	SCKE0
03	SDQ1	45	/SCS2	87	SDQ33	129	*/SCS3
04	SDQ2	46	SDQM2	88	SDQ34	130	SDQM6
05	SDQ3	47	SDQM3	89	SDQ35	131	SDQM7
06	Vcc	48	NC	90	Vcc	132	*SA13
07	SDQ4	49	Vcc	91	SDQ36	133	Vcc
08	SDQ5	50	NC	92	SDQ37	134	NC
09	SDQ6	51	NC	93	SDQ38	135	NC
10	SDQ7	52	*SCB2	94	SDQ39	136	*SCB6
11	SDQ8	53	*SCB3	95	SDQ40	137	*SCB7
12	Vss	54	Vss	96	Vss	138	Vss
13	SDQ9	55	SDQ16	97	SDQ41	139	SDQ48
14	SDQ10	56	SDQ17	98	SDQ42	140	SDQ49
15	SDQ11	57	SDQ18	99	SDQ43	141	SDQ50
16	SDQ12	58	SDQ19	100	SDQ44	142	SDQ51
17	SDQ13	59	Vcc	101	SDQ45	143	Vcc
18	Vcc	60	SDQ20	102	Vcc	144	SDQ52
19	SDQ14	61	NC	103	SDQ46	145	NC
20	SDQ15	62	*Vref	104	SDQ47	146	*Vref
21	*SCB0	63	*SCKE1	105	*SCB4	147	*REGE
22	*SCB1	64	Vss	106	*SCB5	148	Vss
23	Vss	65	SDQ21	107	Vss	149	SDQ53
24	NC	66	SDQ22	108	NC	150	SDQ54
25	NC	67	SDQ23	109	NC	151	SDQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/SWE	69	SDQ24	111	/SCAS	153	SDQ56
28	SDQM0	70	SDQ25	112	SDQM4	154	SDQ57
29	SDQM1	71	SDQ26	113	SDQM5	155	SDQ58
30	/SCS0	72	SDQ27	114	*/SCS1	156	SDQ59
31	NC	73	Vcc	115	/SRAS	157	Vcc
32	Vss	74	SDQ28	116	Vss	158	SDQ60
33	SA0	75	SDQ29	117	SA1	159	SDQ61
34	SA2	76	SDQ30	118	SA3	160	SDQ62
35	SA4	77	SDQ31	119	SA5	161	SDQ63
36	SA6	78	Vss	120	SA7	162	Vss
37	SA8	79	*SCLK2	121	SA9	163	*SCLK3
38	SA10/AP	80	NC	122	SBA0	164	NC
39	SBA1	81	NC	123	SA11	165	EA0
40	Vcc	82	SDA	124	Vcc	166	EA1
41	Vcc	83	SCL	125	*SCLK1	167	EA2
42	SCLK0	84	Vcc	126	*SA12	168	Vcc

*** Please refer Block Diagram**

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0~4.6	V
Voltage on V_{DD} supply to Vss	V_{DD}, V_{DDQ}	-1.0~4.6	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%,	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C	°C-Hr

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	IOH=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	IOL=2mA
Input leakage current (Inputs)	I_{IL}	-2	-	2	uA	3
Input leakage current (I/O pins)	I_{OL}	-3	-	3	uA	3,4

Note: 1. V_{IH} (max) = 5.6V AC .The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC .The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V±200mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (SA_0~SA_{11}, SBA_0~ SBA_1)	C_{IN1}	-	22	pF
Input capacitance (/SRAS, /SCAS, /SWE)	C_{IN2}	-	22	pF
Input capacitance (SCKE0)	C_{IN3}	-	22	pF
Input capacitance (SCLK0)	C_{IN4}	-	28	pF
Input capacitance (/SCS0~/SCS3)	C_{IN5}	-	16	pF
Input capacitance (SDQM0~SDQM7)	C_{IN6}	-	16	pF
Data input/output capacitance (SD0~SD63)	C_{OUT}	-	20	pF
Data input/output capacitance (SCB0~SCB7)	$C_{OUT}1$	-	20	pF

DC CHARACTERISTICS

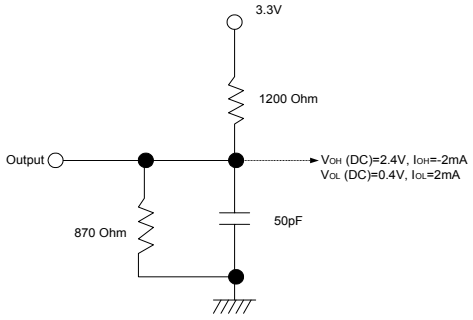
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Value	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA		1,450	mA	1
Precharge Standby Current in power-down mode	I_{CC2}**P**	CKE≤V_{IL}(max), t_{CC}=15ns		20	mA	3
	I_{CC2}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞		20		
Precharge Standby Current in non power-down mode	I_{CC2}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		270	mA	3
	I_{CC2}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		128		
Active Standby Current in power-down mode	I_{CC3}**P**	CKE≤V_{IL}(max), t_{CC}=15ns		90	mA	3
	I_{CC3}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞		90		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		540	mA	3
	I_{CC3}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		360		
Operating Current (Bust Mode)	I_{CC4}	I_{OL}= 0 mA Page Burst t_{CCD} = 2CLKs	3	-	mA	1
			2	1590		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		3,600	mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		28	mA	3

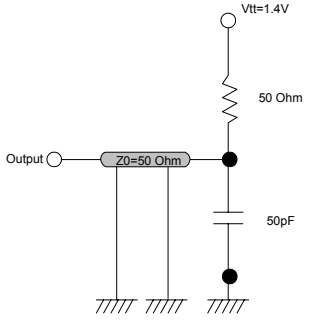
Note:
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive Ics.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Value	Unit	Note
Row active to row active delay		t_{RRD}(min)	20	ns	1
/RAS to /CAS delay		t_{RCD}(min)	20	ns	1
Row precharge time		t_{RP}(min)	20	ns	1
Row active time		t_{RAS}(min)	50	ns	1
		t_{RAS}(max)	100	us	
Row cycle time		t_{RC}(min)	70	ns	1
Last data in to new col. address delay		t_{CDL}(min)	1	CLK	2
Last data in to row precharge		t_{RDL}(min)	1	CLK	2
Last data in to burst stop		t_{BDL}(min)	1	CLK	2
Col. address to col. address delay		t_{CCD}(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Note:
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1CLK earlier than unbuffer DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	Value		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		10			
CLK to valid output delay	CAS latency=3	t_{SAC}	-	6	ns	1, 2
	CAS latency=2		-	6		
Output data hold time	CAS latency=3	t_{OH}	3	-	ns	1, 2
	CAS latency=2		3	-		
CLK high pulse width		t_{CH}	3	-	ns	3
CLK low pulse width		t_{CL}	3	-	ns	3
Input setup time		t_{SS}	2	-	ns	3
Input hold time		t_{SH}	1	-	ns	3
CLK to output in Low-Z		t_{SLZ}	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}	-	6	ns	1
	CAS latency=2		-	6		

Note: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)= 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			SCKEn-1	SCKEn	/SCS	/SRAS	/SCAS	/SWE	SDQM	$SBA_{0,1}$	SA_{10}/AP	SA_0~SA_9, SA_{11}	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (SA_0~SA_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (SA_0~SA_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
SDQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note:

1. OP Code : Operand Code
   SA_0~SA_{11}, SBA_0~SBA_1 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at both banks precharge state.
4. SBA_0~SBA_1: Bank select address.
   If both SBA_0 and SBA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both SBA_0 is "Low" and SBA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both SBA_0 is "High" and SBA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both SBA_0 and SBA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If SA_{10}/AP is "High" at row precharge, SBA_0 and SBA_1 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. SDQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write SDQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read SDQM latency is 2)

Serial Presence Detect Specification

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	Number of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	SDRAM	04
3	Number of Row Addresses on this Assembly	12	0C
4	Number of Column Addresses on this Assembly	10	0A
5	Number of Module Rows on this Assembly	2 rows	02
6	Data Width of this Assembly	72bits	48
7	Data Width of this Assembly	-	00
8	Voltage Interface Standard of this Assembly	LVTTL	01
9	SDRAM Cycle Time @CAS latency of 3	10ns	A0
10	SDRAM Access Time from Clock @CAS latency of 3	6ns	60
11	DIMM configuration type	ECC	02
12	Refresh Rate Type	15.625us/Self Refresh	80
13	Primary SDRAM Width	X8	08
14	Error Checking SDRAM Width	X8	08
15	Min Clock Delay for Back to Back Random Address	tCCD=1CLK	01
16	SDRAM Device Attributes : Burst Lengths Supported	1,2,4,8 & Full page	8F
17	SDRAM Device Attributes : # of banks on SDRAM device	4 bank	04
18	SDRAM Device Attributes : CAS Latency	2,3	06
19	SDRAM Device Attributes : CS Latency	0 clock	01
20	SDRAM Device Attributes : Write Latency	0 clock	01
21	SDRAM Module Attributes	Non-buffered, non-registered & redundant addressing	16
22	SDRAM Device Attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0E
23	SDRAM Cycle Time @CAS Latency of 2	10ns	A0
24	SDRAM Access Time from Clock @CAS Latency of 2	6ns	60
25	SDRAM Cycle Time @CAS Latency of 1	-	00
26	SDRAM Access Time from Clock @CAS Latency of 1	-	00
27	Minimum Row Precharge Time (=t RP)	20ns	14
28	Minimum Row Active to Row Activate (=t RRD)	20ns	14
29	Minimum RAS to CAS Delay (=t RCD)	20ns	14
30	Minimum Activate Precharge Time (=t RAS)	50ns	32
31	Module Row Density	1 rows of 128MB	20
32	Command and Address Signal input Setup Time	2.0ns	20
33	Command and Address Signal input Hold Time	1.0ns	10
34	Data Signal Setup Time	2.0ns	20

35	Data Signal Hold Time	1.0ns	10
36-61	Superset Information	-	00
62	SPD Data Revision Code	Ver 1.2	12
63	Checksum for Bytes 0-62	-	3F
64-71	Manufacturers JEDEC ID Dode per JEP-108E	Transcend	7F, 4F
72	Manufacturing Location	T	54
73-90	Manufacturers Part Number	TS32MLR72V8D2	54 53 33 32 4D 4C 52 37 32 56 38 44 32 20 20 20 20 20
91-92	Revision Code	-	0
93-94	Manufacturing Date	By Manufacturer	Variable
95-98	Assembly Serial Number	By Manufacturer	Variable
99-125	Manufacturer Specific Data	-	0
126	Intel Specification Frequency	100MHz	64
127	Intel Specification CAS# Latency/Clock Signal Support	CL=2, 3 Clock 0	86
128~	Unused Storage Locations	Open	FF